AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please replace the paragraph beginning on page 2, line 4 with the following rewritten paragraph:

- -In this architecture, each cell 10 is controlled by a select cell 18 and a row of select cells 18 is controlled by a select line SELi. Select cells 18 are typically standard transistors (such as n-channel MOS transistors) whose drains are connected to the bit lines BLj, whose sources are connected to the drains of the cells 10 that they control and whose gates are connected to the relevant select line SELi. When a cell, such as cell 10A, is to be accessed, its word line WLi and associated select line SELi are activated as is its bit line BLj. Because select line SELi and word line WLi are activated, the cells of the [[ith]] *ith* row are potentially activated. However, the only cell that will be accessed is cell 10A since only its drain will receive power, through activated select transistor 18A. Other cells that share the accessed word line WLi and select line SELi do not feel any high voltage because their bit lines are not activated. Furthermore, cells sharing the same bit line BLj do not feel the high bit line voltage because their select transistors SELi are off.- -

Please replace the paragraph beginning on page 4, line 1 with the following rewritten paragraph:

- - The present invention is a NOR array having nitride read only memory (NROM) type cells. NROM cells are described in US 5,768,192 and 6,011,725 and in copending US patent ~~application 09/211,981~~ Number 6,552,387, all assigned to the common assignees of the

present invention. The disclosures of the above-identified patents and application are incorporated herein by reference.- -

Please replace the paragraph beginning on page 5, line 15 with the following rewritten paragraph:

- -During the read operation, the presence of the gate and drain voltages V_G and V_D, respectively, induce a depletion layer 54 (Fig. 3B) and an inversion layer 52 in the center of channel 100 (shown in Fig 3A). The drain voltage V_D is large enough to induce a depletion region 55 near drain 104 that extends to the depletion layer 54 of channel 100. This is known as "barrier lowering" and it causes "punch-through" of electrons from the inversion layer 52 to the drain 104.- -

Please replace the paragraph beginning on page 6, line 14 with the following rewritten paragraph:

- - As shown in the exemplary embodiment of Figs. 4A and 4B, the array is segmented and a block k of word lines is accessed through a single common select transistor 122 and a plurality of bit line select transistors 124A and 124B. It will be appreciated that the segmentation is not required to practice the present invention, nor is the particular segmentation shown in Figs. 4A and 4B the only segmentation possible. Exemplary segmentations for a different architecture are described in US Patent ~~Application 09/727,781~~ Number 6,633,496, filed December 4, 2000, whose disclosure is incorporated herein. Such segmentation, which includes multiple levels of select lines, can be utilized herein as well.- -